REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

Rejection of claims 1-4 under 35 U.S.C. § 102(e)

Claims 1-4 presently stand rejected as being anticipated by Kada et al. (U.S. 6,687,321). This rejection is respectfully traversed for the following reasons.

Claim 1 has been amended to more particularly define the present invention. According to amended claim 1, each of the VCDLs has a delay time which corresponds to the voltage control signal. Claim 3 has been similarly amended, now reciting a step of providing a plurality of serial-coupled voltage control delay lines (VCDL) to generate a plurality of oscillating signals according to a voltage control signal, wherein each of the VCDLs has a delay time which corresponds to the voltage control signal.

Support for these amendments is found in the specification at, in particular, page 4, lines 8-10, where it is stated "The delay time Ti(Vc) of each stage is dependent on the common voltage control signal Vc." Accordingly, it is respectfully submitted that no new matter is added.

It is respectfully submitted that each of the delay circuits (IV_0 to IV_N) has a fixed delay time which is not dependent on a voltage control signal. Thus, there is no teaching or suggestion at all in Kada that the delay circuits (IV_0 to IV_N) each have a delay time that is dependent on the voltage control signal.

"A claim is anticipated ***only if each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (emphasis added) Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as complete detail as is contained in the ... claim." (emphasis added) Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The examiner asserts that Kada discloses a "plurality of serial-coupled voltage control delay lines (IV_0-IV_{n+1}). However, Kada lacks any teaching or suggestion at all that the delay circuits (IV_0-IV_{n+1}) ***each*** have a delay time that is ***dependent on a voltage control signal***. With specific reference to claim 2, the examiner states that Kada discloses "that the voltage control delay lines (IV_0-IV_{n+1}) includes a control terminal (necessarily present from 20 to 13) for receiving the voltage control signal (output of 20)." However, all that is shown (and all that is necessary according to Kada's specification) is an output from the "DELAY/CAPACITANCE CONTROLLER" 20 directed to the variable capacitor 13, but not to any part of any of the delay circuits (IV_0-IV_{n+1}).

What is taught by Kada is that "the delay/capacitance controller 20 [...] generates a control signal for selecting the input to the multiplexer 10 [...] and ***controlling the value of capacitance of the variable capacitor*** 13 [...]" (Kada, col. 4, lines 28-34) Thus, from 20 to 13 is a control signal for controlling the value of the variable capacitance. This cannot be interpreted to teach, suggest, or imply that ***each (or any)*** of the VCDLs includes a control terminal for receiving a voltage control signal.

Because Kada fails to teach or suggest voltage control delay lines each having a delay time which corresponds to the voltage control signal, but instead shows only delay circuits having a fixed delay time, Kada does not meet the requirements for an anticipating reference. Therefore, it is respectfully submitted that claims 1 and 3, and their respective dependent claims 2 and 4, are allowable, and withdrawal of the rejection is respectfully requested.

<u>New claims 5-9</u>

Claims 5-9 have been added. Claims 5-9 recites material which is novel and non-obvious in view of the prior art of record, and it is therefore respectfully submitted that claims 5-9 are fully patentable over all the references of record. Support for the new claims is found in the in the original specification at page 5, line 9 to page 6, line 16.

It is respectfully submitted that Kada et al. fails to teach or suggest a voltage control signal that corresponds to a predetermined frequency (an intersection point of the

Curve A and voltage control signal Vc in Fig. 1B), and that the oscillating frequency of the selected oscillating signal is closest to the predetermined frequency. Therefore, applicant asserts that newly added claims 5-9 should be found allowable with respect to the teachings of Kada.

Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-9 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's attorney, the Examiner is invited to contact the undersigned at the numbers shown.

Respectfully submitted,

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Date: January 11, 2006

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